REMARKS

Claim amendments

Claims 1, 5 and 9 have been amended to recite that the low pass filter is continuously coupled to the recited structure. These amendments are supported by the specification, for example figure 2 and the corresponding portion of the specification. No new matter has been added.

Rejection under 35 U.S.C 102

Claims 1-12 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,091,680 to Matsuda. The Applicants respectfully disagree.

Claim 1

In section 2 and 3 of the Action, the Examiner repeatedly asserts that Ref. 10 of Fig. 6 of Matsuda is a "low pass filter". The Applicants strongly disagree. Ref. 10 of Fig. 6 of Matsuda is clearly described as a "level holding circuit", and its operation is precisely recited in column 8, lines 47-61: "*In the level holding circuit 10, when the jump status signal FJUM has a lower level, that is, when the focus servo loop is closed, the switching circuit 1S is closed, and a voltage based on an output of the equalizer is applied over the capacitor 1C. In this case, the selector 9 selects an output of the equalizer, so that the adder 11 can receive the output of the equalizer. On the contrary, when the jump status signal FJUM has a higher level, that is, when the focus servo loop is opened, the switching circuit 1S is opened, so that the voltage charged immediately before the open of the switching circuit 1S is kept over the capacitor 1C. At this time, the selector 9 selects an output from the level holding circuit 10, so that the adder 11 can receive the voltage charged in the capacitor 1C.*"

For ease of understanding, the Applicants have annexed drawings comprising Figs. 1A-A' and Figs. 1B-B' illustrating the operation of level holding circuit 10 as described above and, for comparison purpose, also illustrating the way a low pass filter as described in claim 1 would operate if connected between the equalizer and the adder of Matsuda. Figs. 1A and 1B show the signal (measured in volts) output from the controller (equalizer) over a period of time, wherein the focus servo loop is opened at different points of time t1 and t2 respectively. The signal output from the controller is

assumed to be a sinusoidal wave with amplitude of 0.1V and an oscillating frequency greater than the cutoff frequency of the described low pass filter. This signal is then input to the level holding circuit 10 of Matsuda and the low pass filter as described in the invention (a typical low pass filter, such as LPF 140 in Fig. 2) respectively.

As shown in Fig. 1A', if the focus servo loop is opened at time t1, the signal output from the level holding circuit 10 of Matsuda is (X+0.1) volts because the level holding circuit 10 only has a capacitor for holding the voltage level at the moment when the focus servo loop is opened. Meanwhile, the signal output from the low pass filter as described is X volts rather than (X+0.1), because the low pass filter filters the high frequency component and leaves only the frequency component that is lower than its cutoff frequency. If the cutoff frequency of the low pass filter is small enough, the signal output from the low pass filter contains only the DC component of the signal output from the controller (X volts in this example). Similarly, as shown in Fig. 1B', if the focus servo loop is opened at time t2, the signal output from the level holding circuit 10 of Matsuda becomes (X-0.1) volts as the level holding circuit 10 holds the voltage level at the moment when the focus servo loop is opened. In this circumstance, the signal output from the low pass filter as described is still X volts rather than (X-0.1) volts. That is to say, the capacitor in the level holding circuit only holds the voltage level of the signal output from the equalizer at the moment when the focus servo loop is opened. The low pass filter is used to filter the high frequency component and therefore remains the low frequency component of the signal output from the equalizer, rather than the instantaneous voltage level of the signal. This difference inherently exists between a level holding circuit and a typical low pass filter. The Applicants submit that it is clear from the above that, the level holding circuit 10 disclosed by Matsuda is different from a low pass filter and cannot read on the low pass filter as described in the invention.

Specifically, the Examiner asserts that circuit 10 discloses "a low pass filter for receiving the focusing control signal and producing a layer distance balancing signal". The Applicants note that in Matsuda, the signal generated by the equalizer is not always fed into the capacitor of the level holding circuit 10 since the switch 1S disconnects the two circuits during the opening of the focus servo loop. Therefore, Matsuda cannot be deemed to disclose *"a low pass filter for continuously receiving the*

focusing control signal and producing a layer distance balancing signal", as recited in claim 1. The Applicants further note that it is plain from column 8, lines 47-61 of Matsuda, as well as from figure 6 of Matsuda, wherein selector 9 and switch 1S are controlled by a same signal FJUMP, that should switch 1S be operated so that capacitor 1C of circuit 10 receives continuously the output from the equalizer, selector 9 would never connect the output of circuit 10 to adder 11, and the "layer distance balancing signal" output by circuit 10 according to the Examiner would never be provided to adder 11, so that Matsuda would not disclose a driving device that *"receives a kicking signal and the layer distance balancing signal"* as recited in claim 1. The Applicants submit that only a hardware modification of the circuit disclosed by Matsuda would have allowed circuit 10 to continuously receive the output from the equalizer and produce a "layer distance balancing signal" and to supply the "layer distance balancing signal" to adder 11. No such hardware modification is disclosed or suggested in Matsuda.

At least in view of the above, the Applicants submit that claim 1 is patentable over Matsuda. Should the Examiner insist on calling the level holding circuit 10 of Matsuda a low pass filter, the Applicants respectfully request him to clearly and specifically point out where Matsuda shows the above features, in accordance with 37 C.F.R. 1.104(c)(2).

Claims 5 and 9

The above arguments with regard to claim 1 can be used to show that Matsuda fails to disclose or suggest an optical drive comprising *"a low pass filter for continuously receiving the focusing control signal and producing a layer distance balancing signal"* as recited in claim 5, or a method of controlling an optical drive with a low pass filter and comprising the step of *"continuously sending the focusing control signal to the low pass filter to produce a layer distance balancing signal"* as recited in claim 9, and submit that claims 5 and 9 are patentable over Matsuda.

Claims 2-4, 6-8 and 10-12

Claims 2-4 depend on claim 1, claims 6-8 depend on claim 9 and claims 10-12 depend on claim 9. The Applicants submit that claims 2-4, 6-8 and 10-12 are patentable over Matsuda at least in view of their dependency.

* * *

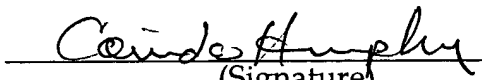
In view of the above, Applicants submit that the application is now in condition for allowance and respectfully urge the Examiner to pass this case to issue.

The Commissioner is authorized to charge any additional fees that may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

March 8, 2005
(Date of Transmission)

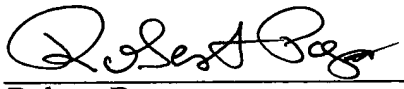
Corinda Humphrey
(Name of Person Transmitting)


(Signature)

March 8, 2005
(Date)

Attachments: Annexed Figs 1A, 1A', 1B, 1B'

Respectfully submitted,



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ANNEX DRAWINGS

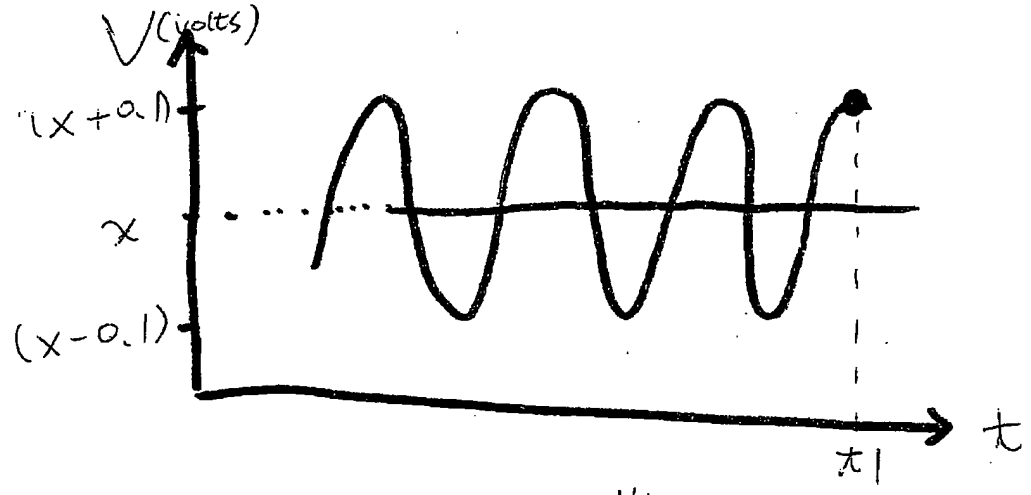

fig 1A

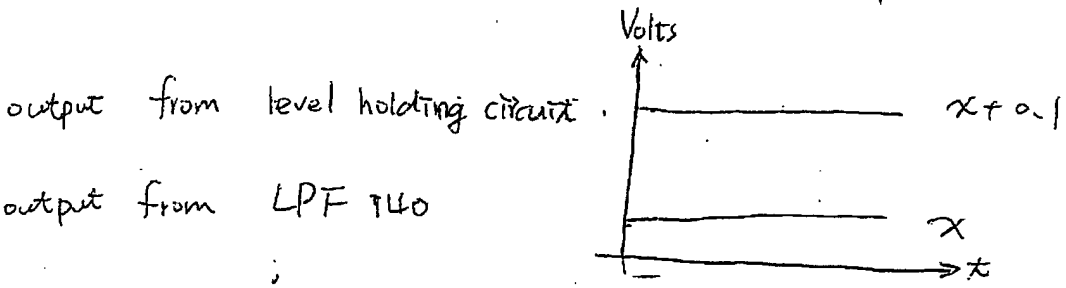

fig. 1A'

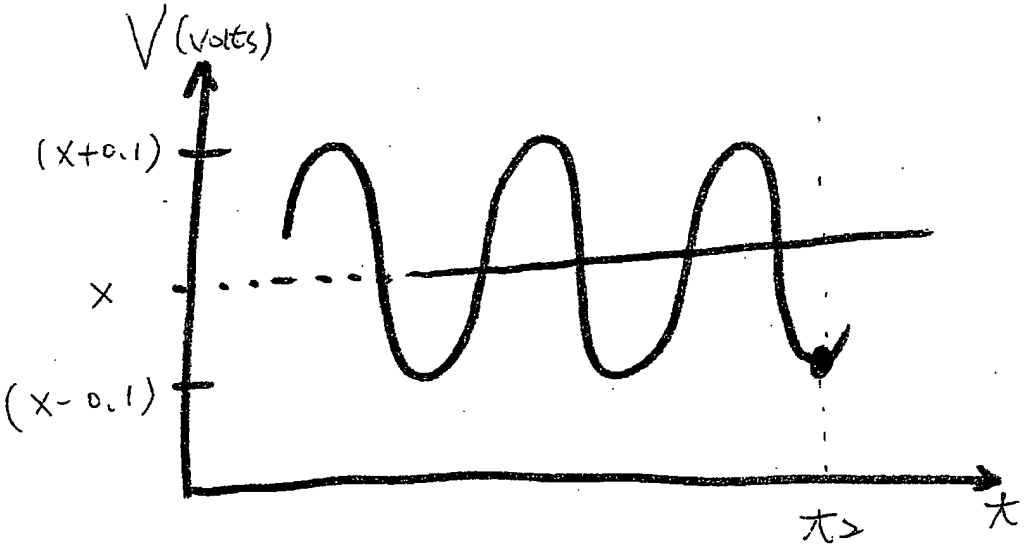

fig 1B

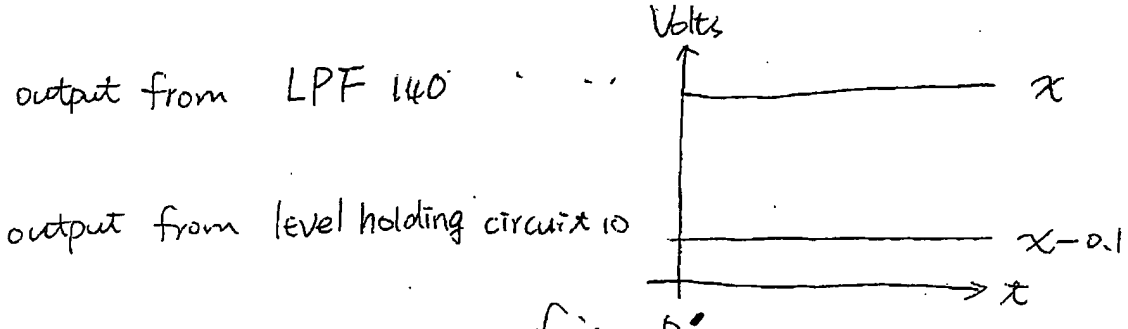

fig. 1B'